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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,350	12/20/2001	Darin A. Chan	50432-528	5761

7590 12/10/2003

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,350	CHAN ET AL.	
	Examiner	Art Unit	
	Dao H Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with th correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-12,14-16 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-12,14-16 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. In response to the communications dated 10/14/2003 through 11/17/2003, claims 2-12,14-16 and 18 are active in this application as a result of the cancellation of claims 19, 20.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Cancellation of claims 19-20. Affirmation of this cancellation was made in the Amendment dated 10/14/2003 and 11/17/2003, and made of record as Paper No. 1103.

Remarks

3. Applicant's argument(s), see Paper No. 1103, filed 11/17/2003, with respect to claim(s) 2-12,14-16 and 18, have been fully considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claim(s) 2-10, 14, and 16 is/are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,537,891 to Dennison et al.

Regarding claim 14, Dennison discloses a method of manufacturing a semiconductor device, as shown in figures 1-6, comprising the steps of:

providing a silicon layer 14 over an insulating layer 12, the silicon layer 14 including a first portion (right portion, or Chip Memory Array Region) and a second portion (left portion, or Chip Periphery Region);

partially removing the first portion of the silicon layer 14, wherein a thickness of the second portion (left portion) is greater than a thickness of the first portion (right portion) (see column 5, lines 46-55 and figs. 2-5); and

forming a first transistor (Access Transistor) in the first portion and a second transistor (Peripheral Transistor) in the second portion, wherein

the first transistor includes first source/drain regions 50 and the second transistor includes second source/drain regions 80, and a depth of the second source/drain regions greater than a depth of the first source/drain regions (see fig. 6). See also column 5, line 24 to column 6, line 57.

Regarding claim 2, Dennison discloses the method wherein the first and

second portions of the silicon layer 14 initially have the same thickness. See figure 1.

Regarding claim 3, Dennison discloses the method wherein the step of partially removing the first portion of the silicon layer includes etching the first portion. See column 5, lines 46-55, and figs. 2-5.

Regarding claim 4, Dennison discloses the method wherein the step of partially removing the first portion of the silicon layer includes depositing a resist over the silicon layer and exposing and developing the resist to expose the first portion of the silicon layer. See column 4, line 28 to column 5, line 55.

Regarding claim 5, Dennison discloses the method comprising all claimed limitations. Note that this is inherent because all etching process must be stopped in a certain amount of time.

Regarding claim 6, Dennison discloses the method wherein the step of partially removing the first portion of the silicon layer 14 includes oxidizing the first portion of the silicon layer and removing the oxidized silicon. See column 4, line 28 to column 5, line 55.

Regarding claim 7, Dennison discloses the method wherein the step of partially removing the first portion of the silicon layer 14 includes depositing a mask layer and a

resist over the silicon layer 14 and exposing and developing the resist to expose a portion of the mask layer over the first portion of the silicon layer 14and removing the mask layer over the first portion of the silicon layer. See column 4, line 28 to column 5, line 55.

Regarding claim 8, Dennison discloses the method further comprising the step of removing the mask layer. See column 5, lines 5-55.

Regarding claims 9 and 10, Dennison discloses the method wherein the mask layer is an antireflective material, or a silicon nitride. See column 4, lines 28-67.

Regarding claim 16, Dennison discloses a semiconductor device, as shown in figures 1-6, comprising:

a insulating layer 12;

a silicon layer 14 over the insulating layer 12, the silicon layer 14 including a first portion (right portion, or Chip Memory Array Region) and a second portion (left portion, or Chip Periphery Region); and

a first transistor (Access Transistor) is formed in the first portion and a second transistor (Peripheral Transistor) is formed in the second portion,

wherein a thickness of the second portion is greater than a thickness of the first portion (see column 5, lines 46-55 and figs. 2-5), and the first transistor includes first source/drain regions 50 and the second transistor includes second source/drain regions

80, and a depth of the second source/drain regions 80 greater than a depth of the first source/drain regions 50 (see fig. 6). See also column 5, line 24 to column 6, line 57.

Claim Rejections - 35 U.S.C. § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim(s) 11-12, 15, and 18 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,537,891 to Dennison, in view of the following remarks.

Regarding claims 11 and 12, Dennison discloses all the claimed limitations. Except for isolating features. However, it would have been well known in the art that isolating features such as shallow trench isolation are usually formed between semiconductor devices to isolate one device from the other. It is further note that it is obvious to one of ordinary skill in the art that isolating features could be formed either before or after the partially removal of the first portion of the silicon layer since it is obvious that any of such order of forming the isolating features would not make any change in the spirit and scope of the invention of Dennison.

Regarding claims 15 and 18, Dennison discloses the semiconductor device comprising all claimed limitations, except for the diffusivity of the second dopant into silicon is greater than the diffusivity of the first dopant into silicon. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the diffusivity of the second dopant into silicon could be greater than, less than, or equal to the diffusivity of the first dopant into silicon since applicant has not disclosed that such diffusivity of the second dopant into silicon being greater than that of the first dopant into silicon solves any stated problem or is for any particular purpose, and it appears that the invention of Dennison would perform equally well with the diffusivity of first dopant and the second dopant being either the same or different.

Conclusion

8. **THIS ACTION IS MADE FINAL.** A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao Nguyen whose telephone number is (703) 305-1957 (before January 08, 2004), or (571)272-1791 (after January 08, 2004). The examiner can normally be reached on Monday-Friday 9:00am - 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910 (before January 08, 2004), or (571)272-1787 (after January 08, 2004). The fax numbers for all communication(s) is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
November 20, 2003